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k-Space Associates

Understanding the wafer carrier

contents

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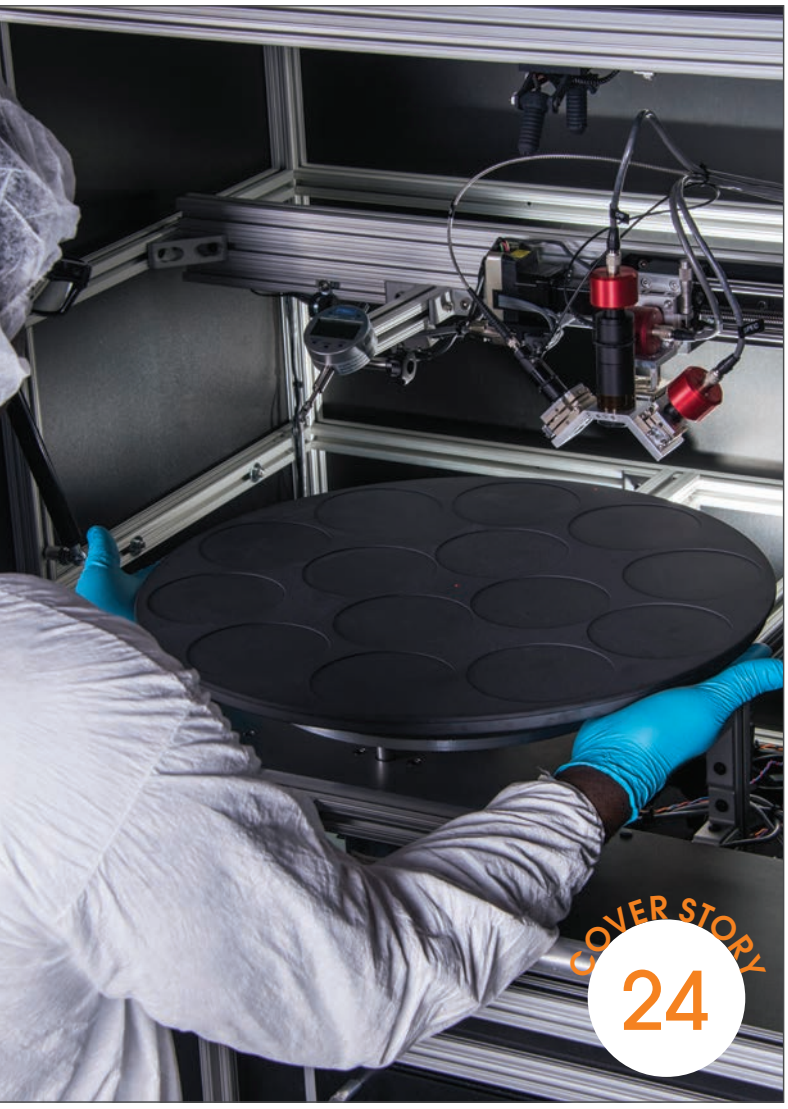
features



Refining chip manufacturing with wafer carrier monitoring

Mapping a carrier's emissivity and temperature profile exposes microcracks and emissivity variations that can directly impact thin-film deposition and device performance

BY CARRIE ANDRE AND DARRYL BARLETT FROM K-SPACE ASSOCIATES

A KEY PROCESS in the manufacture of most compound semiconductor chips is epiwafer growth. Engineers with expertise in this area are highly valued because they can ensure high yields, develop new devices quickly, and help diagnose faults within the reactor. Their skills are not limited to knowing the best growth rates and temperatures for depositing various alloys, but extend to understanding how to treat the hardware to obtain the best run-to-run and tool-to-tool repeatability.

If these engineers are responsible for producing epiwafers in an MOCVD reactor, they will have had to also devise an approach for minimizing variations associated with wafer carriers. Also known as platens or susceptors, these hardware components, which accommodate substrates during the deposition process, are typically baked in an oven after every growth run for many hours – and sometimes for several days.

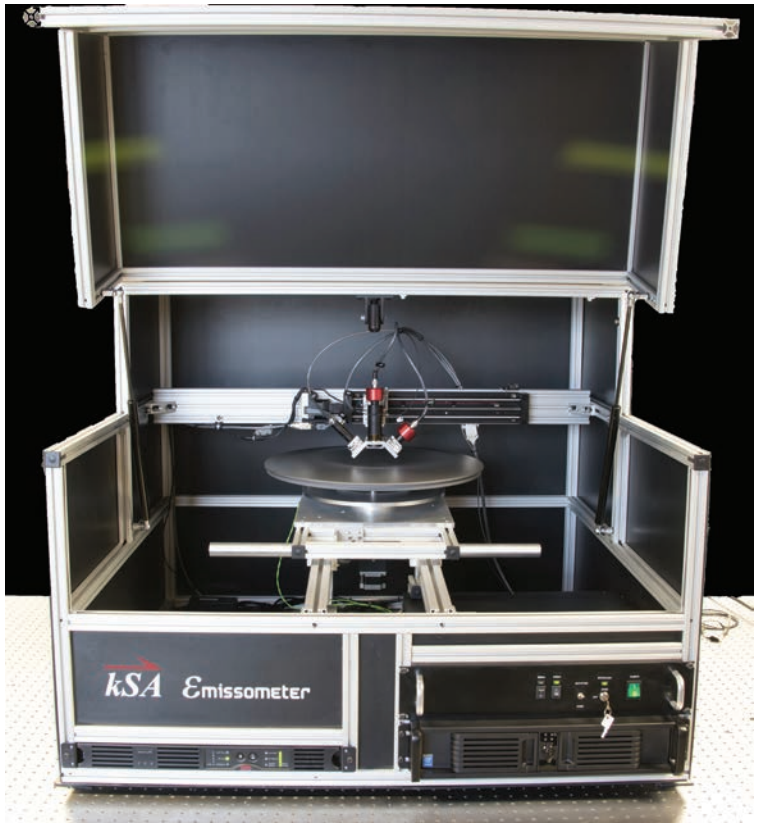


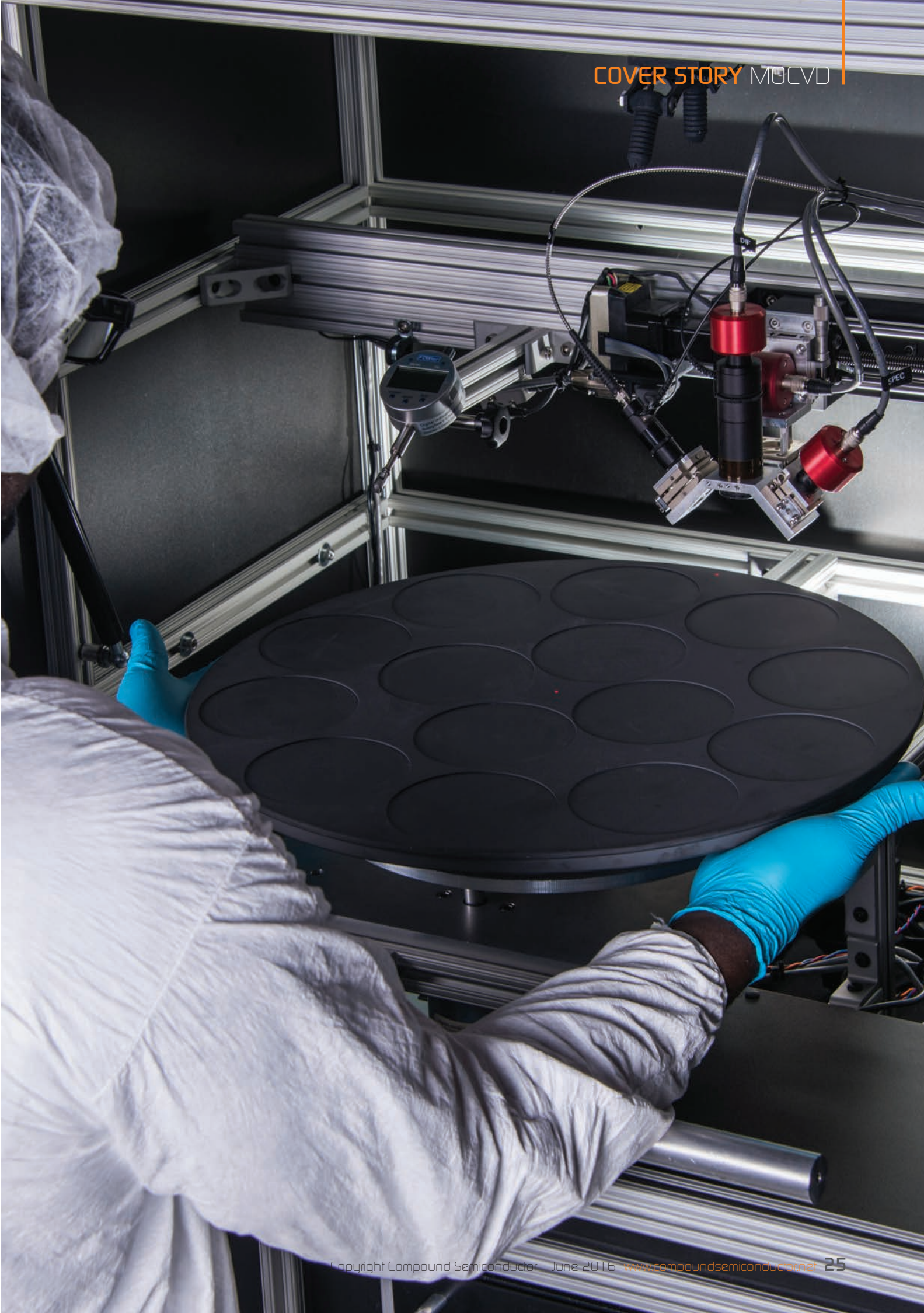
Figure 1. The kSA Emissometer, with its lid open, measuring the emissivity of a loaded Veeco K465i carrier.

The aim of this bake is to remove deposited material from the carrier, and rid it of any contamination. Ideally, the carrier is cleaned so that its emissivity – that is, its emission of infrared energy that heats the substrate to the required growth temperature – is returned to its original value. By doing this, the same recipe can be used from one run to the next to produce layers with the same thickness and composition.

While this may sound easy, in practice it is not. Multiple growth runs and subsequent bakes change the uniformity of carrier emissivity. And complicating matters further, the MOCVD chipmakers do not have a quantitative method for monitoring these carrier changes. Process engineers in many MOCVD fabs are forced to accept the changes in emissivity, and account for them by making small adjustments to the temperature set point, based on the growth history for a particular carrier. Although this helps, it can only address changes in the average emissivity, and it cannot compensate for any non-uniformities that may arise.

Another tough call for any MOCVD process engineer is to determine when it is no longer appropriate to use a carrier. One way to do this is to visually inspect a carrier and discard it if it contains significant defects or blemishes. Alternatively, the wafer carrier can be retired after the material grown on it exceeds a certain limit.

Unfortunately, both options are heavily flawed. Downsides include wasted growth runs, yield reduction, significant reactor downtime due to catastrophic carrier failure, and a very limited provision of the quality control data needed for improving the process for determining end-of-life.



These issues can be illustrated by considering the SiC growth process. When a carrier is coated with this material, microcracks can appear in the film that eventually cause the carrier to be unusable. These cracks are typically invisible to the naked eye, and result from a small mismatch between the coefficient of thermal expansion of the wide bandgap SiC semiconductor and that of graphite, which is the bulk material of the carrier. The cracks arise due to frequent, large-scale temperature swings during the MOCVD deposition process as well as extreme baking conditions.

The cracks in the SiC coating are not there when the carrier has just been introduced, but start to appear when the thickness of the film exceeds around 100 μm. These imperfections are incredibly detrimental, because the exposed graphite promotes carbon doping, and the microcracks significantly change surface emissivity and can ultimately cause implosion of the carrier inside the reactor. It is of little surprise, then, that many wafer carriers are retired after completing a set number of growth runs. But if engineers err too far on the side of caution, the carrier may be laid to rest too soon. The crux of the issue is that the 'real' lifetime of a particular carrier tends to be a mystery.

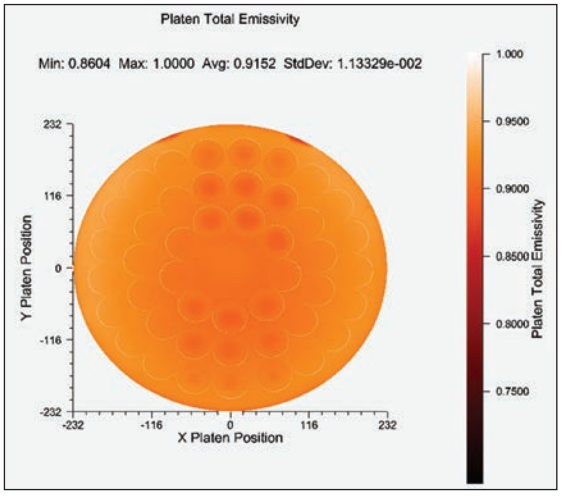


Figure 2. An emissivity map produced by the kSA Emissometer. The darker areas are the wafer pockets in the wafer carrier.

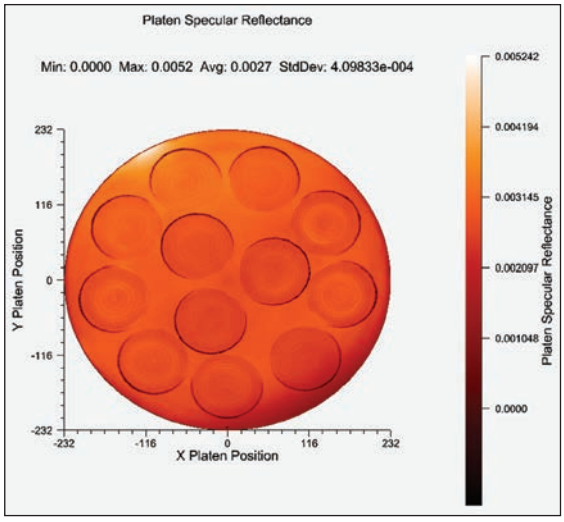


Figure 3. A specular reflectance map produced by the kSA Emissometer uncovers pocket machining marks in the MOCVD carrier.

Carrier inspection

To offer some insight into this crucial issue, our team from k-Space Associates of Dexter, MI, has developed an *ex-situ* instrument for measuring carrier emissivity (see Figure 1). The kSA Emissometer measures, over the entire carrier, absolute diffuse and specular reflectance. Summing together both of these reveals the total emissivity over the entire carrier.

Our tool can provide emissivity maps with a spatial resolution of 0.5 mm. This level of fidelity exposes non-uniform pocket emissivities, which can result from partial loading of the carrier during process development. This is the case for the carrier mapped in Figure 2, where pockets loaded with wafers were consequently protected from MOCVD deposition. The upshot is surface properties in those areas that were far closer to those of the original, new carrier.

When a wafer carrier is properly baked, the main contributor to total emissivity is the diffuse reflectance component. Meanwhile, the specular component is expected to remain at or close to zero over the entire surface. But when there is residual MOCVD deposition on the carrier, the situation is markedly different, with spikes appearing in the specular reflectance signal.

Specular reflection is also capable of exposing other forms of imperfection, such as the pin-pointing of small irregularities on the carrier surface. Our tool, for example, can uncover machining marks underlying the SiC coating (see Figure 3).

Another feature of our instrument is its capability to average total emissivity over certain radii – this can correspond to the location of optical pyrometers (such as RealTemp, EpiTT, and our own kSA ICE instrument). Armed with this insight, engineers can fine-tune the temperature set points for a production run with a particular carrier. This approach yields more accurate results than the 'estimation' methodologies widely employed today.

To underline the capability of *ex-situ* emissivity characterization, we have proven the strong correlation between the carrier emissivity and the actual carrier temperature in an MOCVD reactor. This has been accomplished by comparing carrier emissivity mapping, using the kSA Emissometer, with carrier temperature mapping using the kSA ScanningPyro (the latter is shown in Figure 4).

This study began with the selection, by a chip manufacturer, of an in-production carrier. We visually inspected this (see Figure 5 for a photograph of its central portion), before scanning it with a kSA Emissometer. The emissometer unveiled microcracks that are not visible to the naked eye. They produce a different emissivity, and should result in temperature non-uniformity on the heated carrier (see Figure 6 (a)).

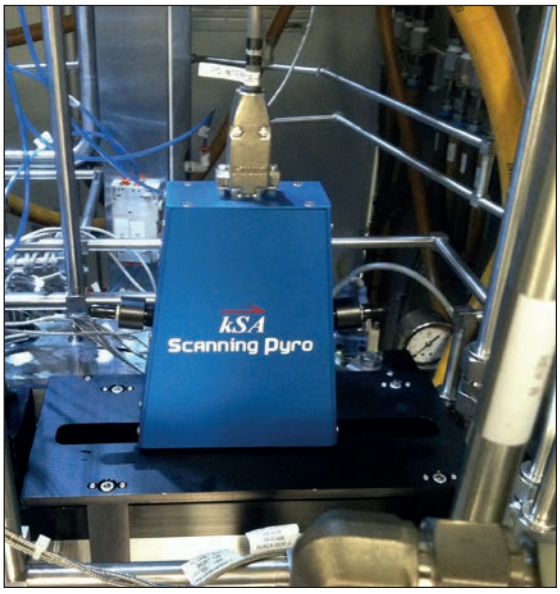


Figure 4. The kSA Scanning Pyro, in use on a Veeco K465i MOCVD reactor.

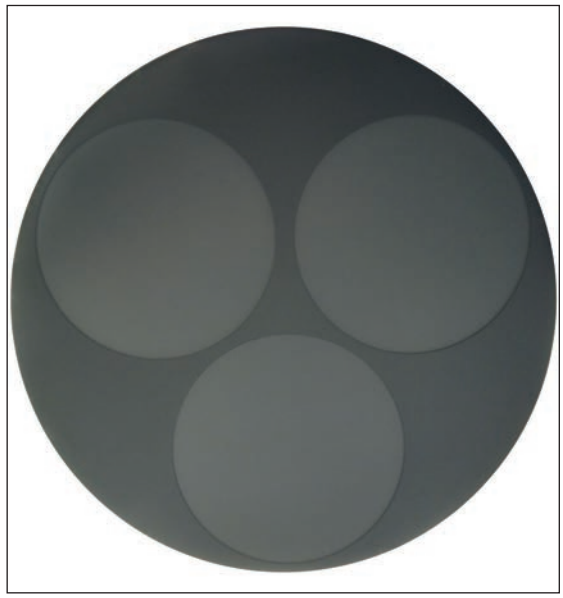


Figure 5. A photograph of an in-production wafer carrier used in trials conducted by k-Space Associates. This image shows what the human eye and the digital camera can – and cannot – see during inspection of a carrier. Microcracks are present on the carrier, but are not unveiled in this image.

We loaded this in-production carrier into a Veeco K465i, and heated the reactor to a temperature of 1000°C, according to a pyrometer in the middle of the chamber. Further inspection of the carrier came from our *in-situ* ScanningPyro tool – it is a dual-detector pyrometer with full scanning capability that can yield full carrier temperature maps in a single scan, and ultimately determine the temperature uniformity of the carrier.

Microcracks are also exposed in the temperature maps produced by our *in-situ* ScanningPyro (see Figure 6 (b)). In addition to this imperfection, the mapping shows that the centre of the carrier is by far its coolest part. This is expected, due to the cooler spindle beneath the centre of the carrier.

Our study underlines how our emissometer complements the scanning pyrometer. What's more, it shows how our emissometer – which opens the door to a scientifically based, quantitative approach to wafer carrier characterization in the production environment – is well positioned to become an indispensable tool for a variety of tasks. It can be used to determine the quality of a carrier bake after a deposition run, and ultimately eliminate guesswork from making a 'go-no-go' decision on the suitability of a particular carrier for the next production run. It can also deliver an accurate value for surface emissivity, aiding temperature set-point adjustments for a particular wafer carrier following a bake. And our emissometer can also: uncover microcracks, evaluate their severity, and help an engineer to decide when to retire a wafer carrier at the end of its useful lifetime; qualify wafer carrier vendors, via examination of the emissivity uniformity over the carrier, and within the batch of carriers; provide incoming quality control of the new wafer carriers; and prevent wasted MOCVD growth runs.

In short, the kSA Emissometer is a highly capable tool that enables engineers to drive up throughput and yield by offering unique insights into the condition of the wafer carrier.

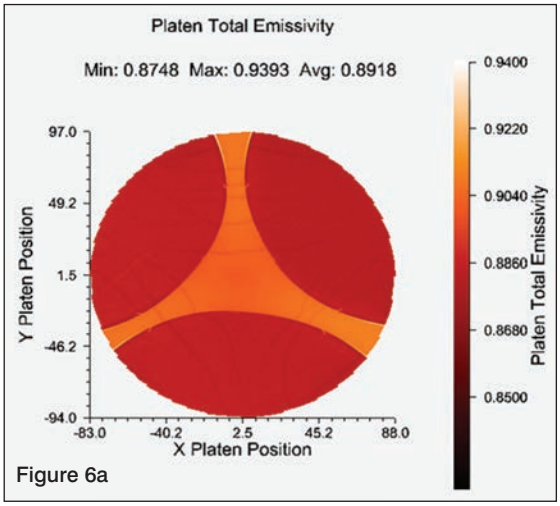


Figure 6a

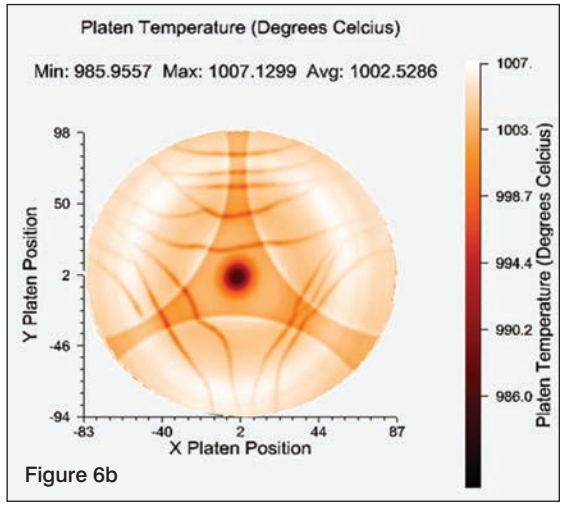


Figure 6b

Figure 6. (a) The kSA Emissometer unveils microcracks when generating a map of the total emissivity of a Veeco k465i wafer carrier (b) The microcracks are also seen in a map produced by the kSA Scanning Pyro *in-situ* instrument.